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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/422,887 10/21/99 FOGAL

R 95-0134.05

EXAMINER

MMC2/0524

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DAVIS, J

ART UNIT

PAPER NUMBER

2822

DATE MAILED:

05/24/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/422,887

Applicant(s)

FOGAL ET AL.

Examiner

J. L. Davis

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- 1) ☒ Responsive to communication(s) filed on 21 October 1999.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 7-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 7-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 October 1999 is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some * c) ☐ None of the CERTIFIED copies of the priority documents have been:
- 1) ☐ received.
 - 2) ☐ received in Application No. (Series Code / Serial Number) _____.
 - 3) ☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.

- 18) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: _____.

DETAILED ACTION

This office action is in response to application papers filed 10/21/99.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 58 (p. 7, line 10) and 60 (p. 7, line 11). Correction is required.

Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect can be deferred until the application is allowed by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7, 9-11 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Farnworth (5,012,323).

Re claim 7, Farnworth teaches a method of stacking a plurality of die including the steps of mounting an upper die (41) on a lower die (43) and defining a minimum angular offset with said mounting, wherein said minimum angular offset allows access

to a bonding site (46) on the lower die (43). See Figs. 4 and 5 and col. 4, line 36 through col. 5, line 20.

Re claims 9-11, Farnworth teaches the steps of stacking all of the dies, wherein said stacking defines an offset angle with any two of the dies and, after stacking, bonding wire (47) to the dies (col. 4, lines 65-68).

Re claim 17, Farnworth teaches the steps of serially stacking all the dies (41, 43) and establishing a unique orientation for each die of said all dies (41, 43), wherein said orientation for each die defines an underlying bond pad clearance.

Claims 7-12 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakurai (JP 57-31166A).

Re claim 7, Sakurai teaches a method of stacking a plurality of die (1a-1d) including the steps of mounting an upper die (1d) on a lower die (1c) and defining a minimum angular offset with said mounting, wherein said minimum angular offset allows access to a bonding site (2c) on the lower die (1c). See Figs. 2a and 2b and the second and third paragraphs of p. 4 of the translation.

Re claim 8, Sakurai teaches the step of mounting a lowest die (1a) on a substrate (4). See Fig. 3.

Re claims 9-11, Sakurai teaches the steps of stacking all of the dies (1a-1d), wherein said stacking defines an offset angle with any two of the dies and, after stacking, bonding wire (7) to the dies (1a-1d).

Re claim 12, Sakurai teaches the steps of stacking the plurality of dies (1a-1d) along an axis, establishing an orientation for each die of said plurality of dies, clearing a line of sight to contact areas of any immediately underlying die with said orientation of said each die, wherein said line of sight is parallel to said axis and clearing said line of sight to contact areas of any underlying die with said orientation of said each die.

Re claim 17, Sakurai teaches the steps of serially stacking all the dies (1a-1d) and establishing a unique orientation for each die of said all dies (1a-1d), wherein said orientation for each die defines an underlying bond pad (2a-2d) clearance.

Claims 7-9 and 12-17 are rejected under 35 U.S.C. 102(b) as being anticipated by de Givry (EP 0,489,643 A1).

Re claim 7, de Givry teaches a method of stacking a plurality of die (14, 16) including the steps of mounting an upper die (16) on a lower die (14) and defining a minimum angular offset with said mounting, wherein said minimum angular offset allows access to a bonding site (18) on the lower die (14). See Fig. 1 and p. 6 of the translation.

Re claim 8, de Givry teaches the step of mounting a lowest die (14) on a substrate (12). See Fig. 2.

Re claim 9, de Givry teaches the steps of stacking all of the dies (14, 16), wherein said stacking defines an offset angle with any two of the dies, and bonding wire (19) to the dies (14, 16).

Re claim 12, de Givry teaches the steps of stacking the plurality of dies (14, 16, 26, 28) along an axis, establishing an orientation for each die of said plurality of dies (14, 16, 26, 28), clearing a line of sight to contact areas of any immediately underlying die with said orientation of said each die, wherein said line of sight is parallel to said axis, and clearing said line of sight to contact areas of any underlying die with said orientation of said each die (see Fig. 3 and p. 7 of translation).

Re claims 13 and 14, de Givry teaches the steps of spiraling the plurality of chips (14, 16, 26, 28) around an axis perpendicular to the plurality of chips (14, 16, 26, 28) and ensuring bond pad clearance to each chip of the plurality of chips (14, 16, 26, 28), wherein spiraling the plurality of chips further comprises spiraling the plurality of chips around an axis passing through each chip (Fig. 3).

Re claims 15 and 16, de Givry teaches that the step of spiraling includes spiraling the plurality of chips around an axis passing through the center of each chip and the step of ensuring bond pad clearance further comprises rotating a chip around the axis at least to the extent that a bond pad on an underlying chip is exposed (Fig. 3).

Re claim 17, de Givry teaches the steps of serially stacking all the dies (14, 16) and establishing a unique orientation for each die of said all dies (14, 16) wherein said orientation for each die defines an underlying bond pad (18) clearance (Fig. 1 and p. 6 of the translation).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. L. Davis whose telephone number is (703) 308-6182. The examiner can normally be reached on M-Th (7:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

J. L. Davis

jld
May 22, 2000

Carl Whitehead, Jr.

**CARL WHITEHEAD, JR.
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